Supporting information for

Operando Observation of Gate Defect in Quantum Dot-Based Field Effect Transistors

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1. FET fabrication and electrical characterization

Figure S 1 illustrates the steps for fabricating the defective FET, with a hole that shorts the gate electrode to the channel. Compared to conventional FET fabrication, an additional lithography step is used to etch a square hole with a 3 μm edge size.

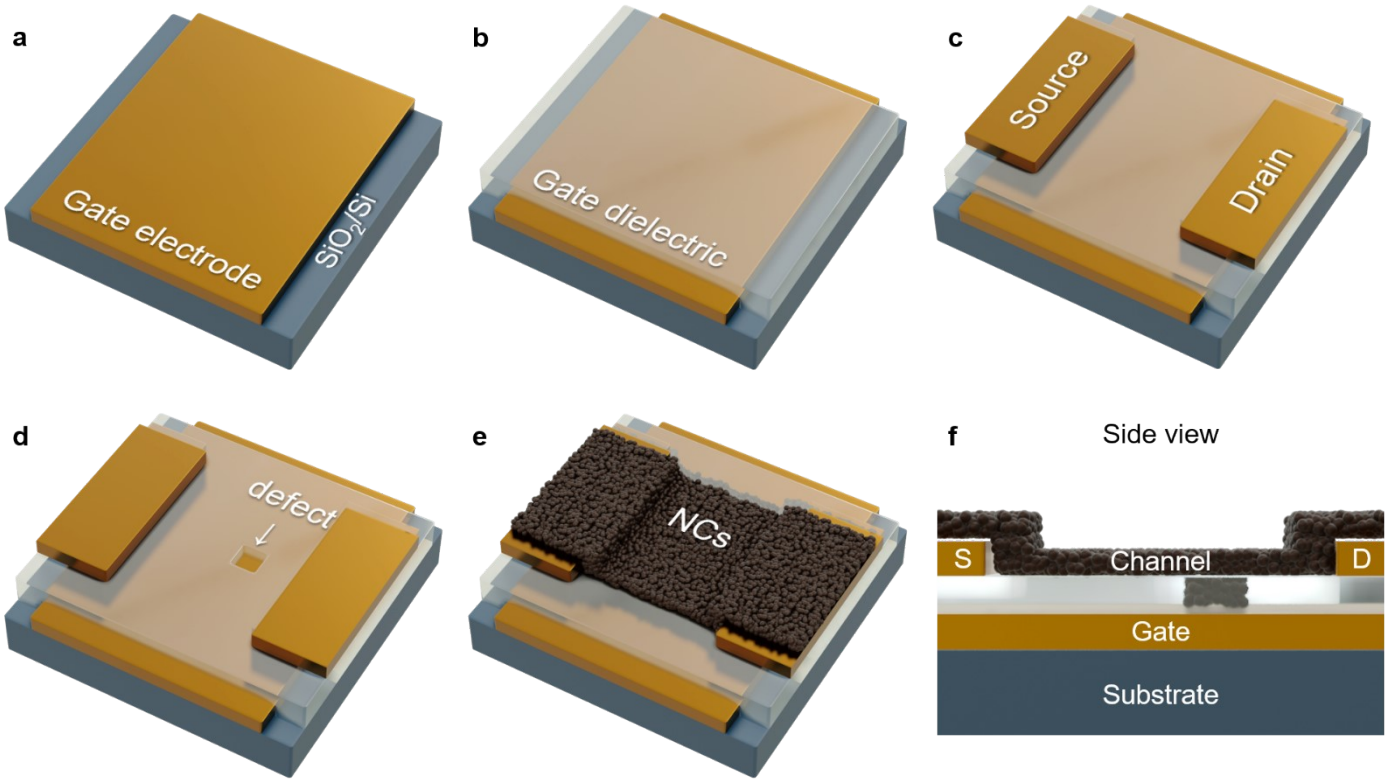

***Figure S 1 Fabrication of the defective FET**. a. Deposition of the back gate electrode. b. Deposition of the alumina used as FET dielectric. c. Deposition of the drain-source electrodes defining the FET channel. d. E-beam lithography step to etch a hole within the dielectric. e. Coating with the HgTe CQD film. f. Side view of the device from part e.*

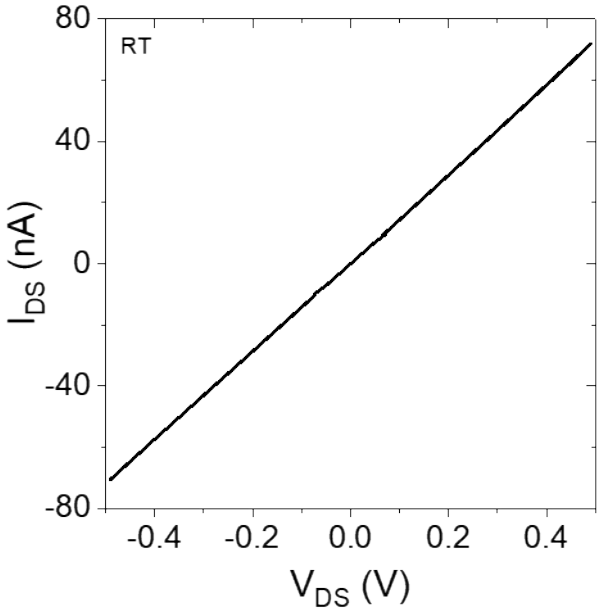

Figure S 2 I-V curve at room temperature for the hole-free conventional FET.

2. XPS imaging

HgTe as a channel film offers the benefit of having two detectable states – Hg 5d at 8 eV and Te 4d at 40 eV binding energy – that can be tracked using a soft X-ray beam operating at 95 eV, see **Figure S 3**.

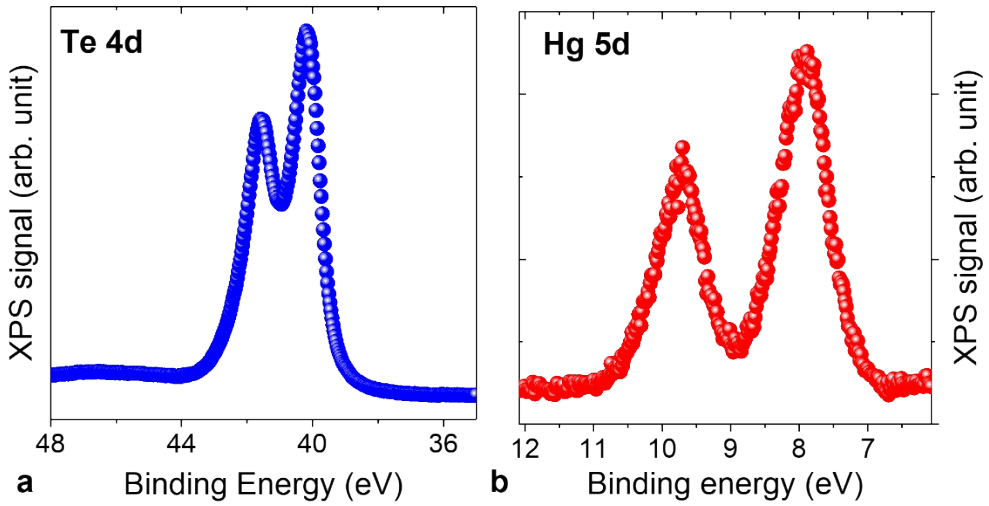

Figure S 3 Low energy core levels from the HgTe CQD film. *a. Spectrum relative to the Te 4d state. b. Spectrum relative to the Hg 5d state.*

The **Figure S 4** depicts the data analysis process, starting from the raw data, where each point of the map is a spectrum, leading to a final map whose scale relates to the bias-induced energy shift.

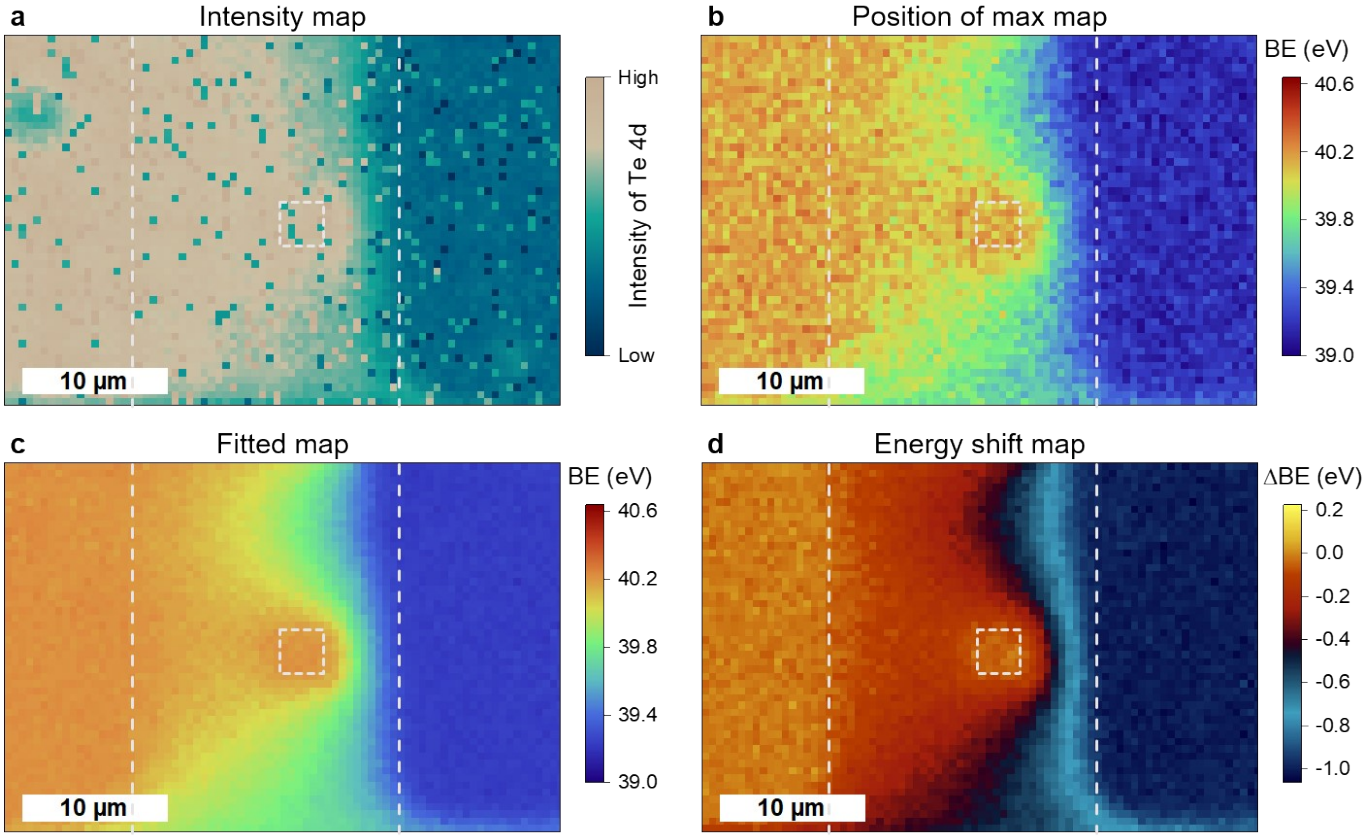

Figure S 4 Data analysis procedure. Data are acquired while V_{DS} = -1 V, V_{GS} = 0 V. a. Map obtained from the integrated intensity of the Te $4d_{5/2}$ component in the Te 4d spectrum. b. Map of the same

area based on the location of the maximum (peak position of Te $4d_{5/2}$) from the Te 4d spectrum, in binding energy. c. Map of the same area based on the Gaussian fitting of the Te 4d doublet to determine the binding energy of the Te $4d_{5/2}$ component. d. Energy shift map obtained by subtracting to the map from part c. the same map acquired with all electrodes grounded. The vertical dashed lines mark the channel boundaries, while the dashed square indicates the location of the hole.

Until breakdown the spectra relative to a core level is mostly sifted (*i.e.,* no broadening, neither new component) by bias application as illustrated in Figure S 5

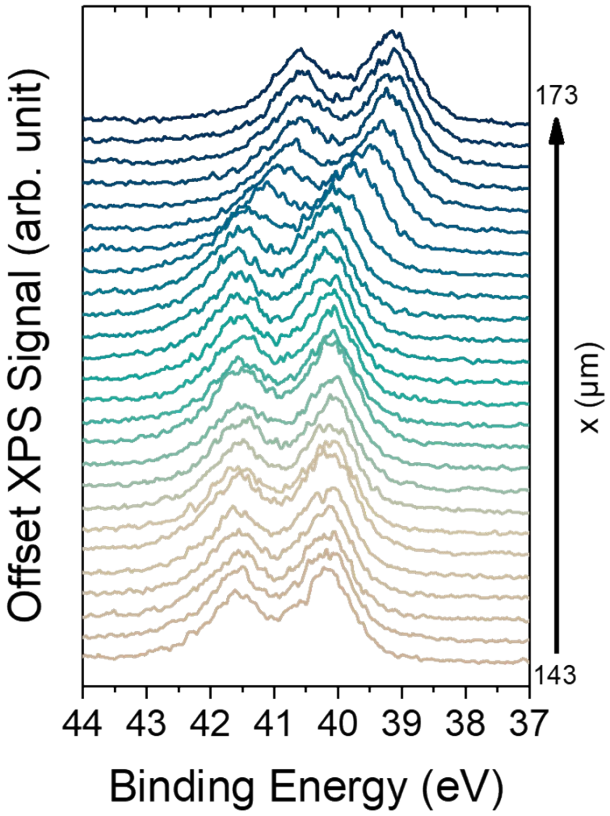

Figure S 5 Spectra relative to the Te 4d state *extracted from the map of Figure S 4, along the x axis and for a y position overlapping with the defect.*

3. Post mortem structural analysis of FET

Sample described in the main text, particularly in Figure 4 of the main text. The main source of damage occurs at the interface between the drain/source electrodes with the gate electrode. Optical microscopy image presents a change of sample color there, which can be further monitored by using energy dispersive X-ray spectroscopy (EDX) at a bias of 10 kV, see **Figure S 5**. We clearly see that Hg element is missing at this interface, while the silicon from the substrate gets more intense. This suggests that the HgTe CQD film has been removed in this region, leaving the substrate exposed. Notably, the area corresponding to the channel appears mostly unaffected.

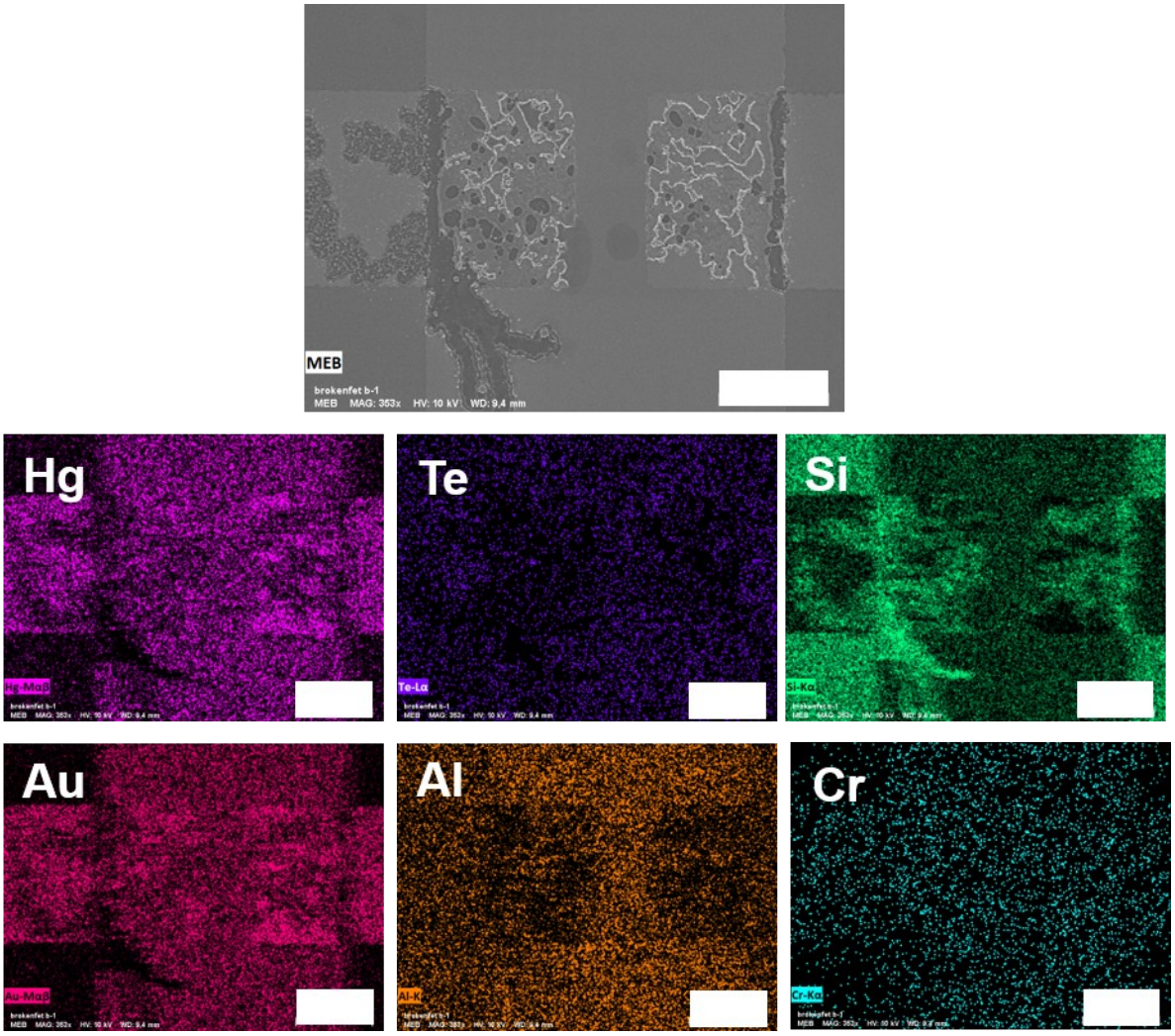

Figure S 6. Post mortem EDX mapping*. (top) SEM image relative to the FET, described in Figure 4 from main text, after its exposure to 40 V gate bias. (bottom) EDX mapping relative to Hg, Te, Si, Au, Al and Cr. All scale bars (white rectangles) are 30 µm long*

When a thin film is deposited as in **Figure S 6**, it has a low resistance and the damage resulting from a high gate voltage application can be different. Not only the gate/drain electrodes are damaged, but the film with the channel is also removed. Such damage makes the inferring of the potential map from XPS impossible due to the absence of material to analyze.

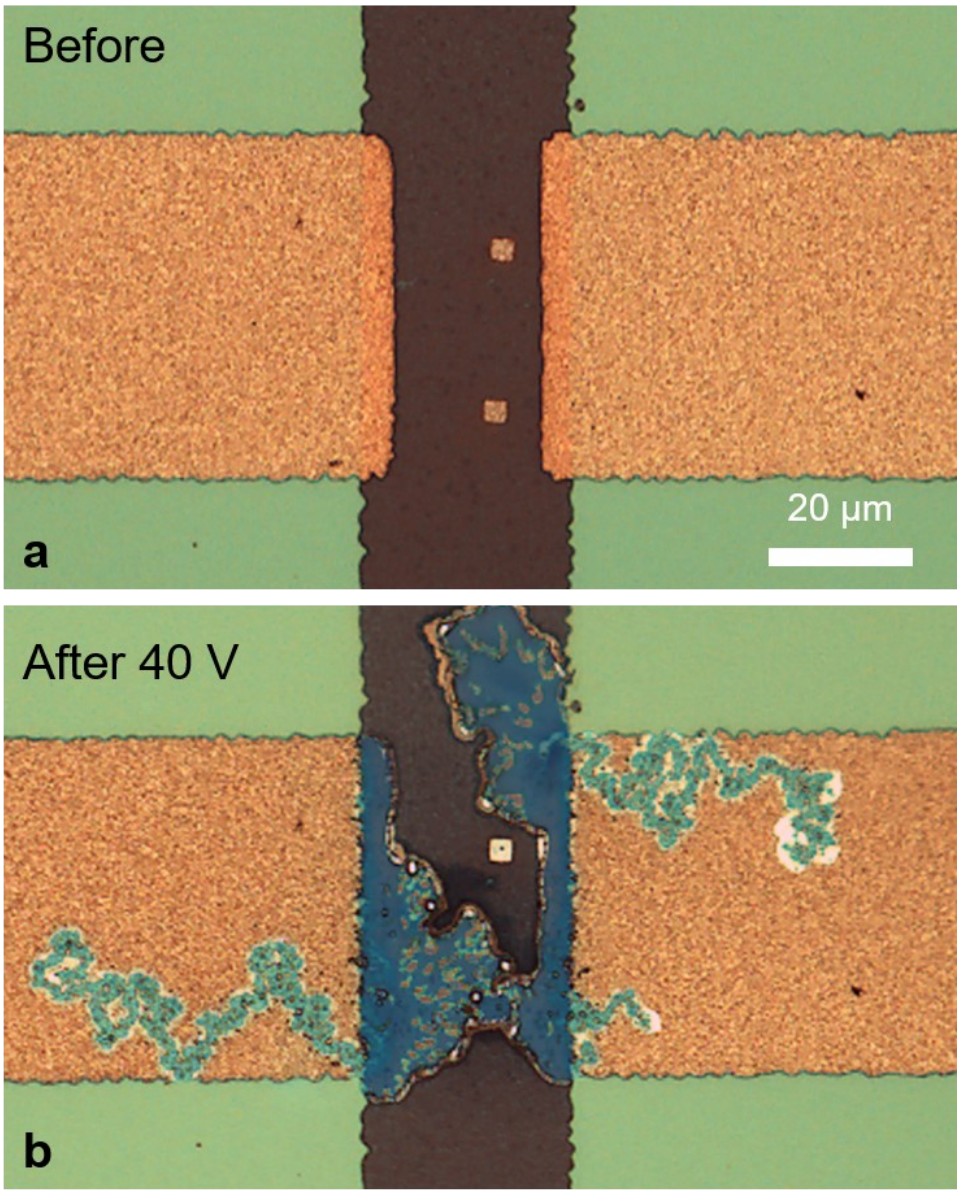

Figure S 7 Imaging from a second FET before and after its exposure to a 40 V gate bias. *a. (resp b.) Optical microcopy image from the channel of a second FET before (resp after) its exposure to a 40 V gate bias. Scale bar is the same for part a and b.*

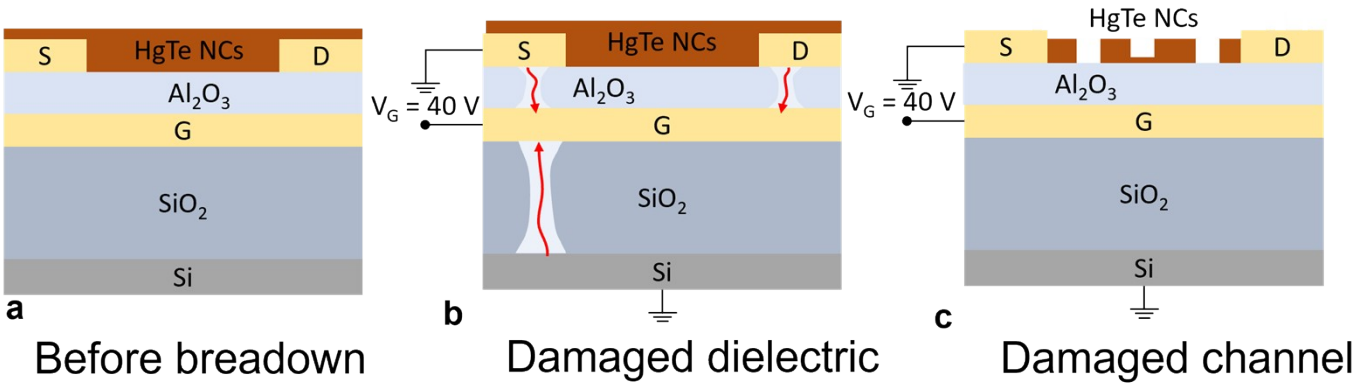

Figure S 8 Schematic of the suggested breakdown mechanisms*. a. Device before breakdown. b. Device damaged via a filamanentation through the dielectric or c. through a removal of the channel.*